CLAIMS:

1. A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different; and

forming a gate line over respective active areas to provide individual transistors, the transistors corresponding to the active areas having the different widths having different threshold voltages.

2. The semiconductor processing method of claim 1 further comprising for the transistors having the different widths, providing the different threshold voltages without using a separate channel implant for the transistors.

3. The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron.

4. The semiconductor processing method of claim 1, wherein the different threshold voltages are each less than 2 volts.

5. The semiconductor processing method of claim 1, wherein the different threshold voltages are each less than 1 volt.

6. The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron, and the different threshold voltages are each less than 2 volts.

7. The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron, and the different threshold voltages are each less than 1 volt.

8. A method of forming a pair of field effect transistors comprising:

forming a pair of active areas over a substrate, one of the active areas having a width less than one micron;

forming a gate line over both active areas to provide a pair of transistors having different threshold voltages, the transistors being provided with the different threshold voltages without using a separate channel implant for either transistor; and

wherein the transistor with the lower of the threshold voltages corresponds to the active area having the width less than one micron.

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9. The method of claim 8 further comprising forming the transistor having the higher of the threshold voltages to have an active area width greater than one micron.

10. The method of claim 8 further comprising forming the transistor having the higher of the threshold voltages to have an active area width less than one micron.

11. The method of claim 8 further comprising conducting only one common channel implant for the pair of transistors.

12. The method of claim 8, wherein the forming of the pair of active areas comprises forming shallow trench isolation regions received within the substrate proximate the active areas.

13. The method of claim 8, wherein the forming of the gate line comprises forming a common gate line over the active areas.

14. The method of claim 8, wherein the forming of the gate line comprises forming a common gate line over the active areas, the transistors being formed in a parallel configuration.

15. A method of forming integrated circuitry comprising fabricating two field effect transistors having different threshold voltages without using a separate channel implant for one of the transistors versus the other.

16. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming at least one active area of one of the transistors to have a width less than one micron.

17. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming both active areas of the transistors to have widths less than one micron.

18. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming both active areas of the transistors to have different widths.

19. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming both active areas of the transistors to have different widths, each of which being less than one micron.

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20. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming shallow trench isolation regions within a substrate proximate the two field effect transistors, the shallow trench isolation regions defining, at least in part, active area widths of the transistors.

21. A semiconductor processing method comprising forming two series of field effect transistors over a substrate, one series being isolated from adjacent devices by shallow trench isolation, the other series having active area widths greater than one micron, the one series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series.

22. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant.

23. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

24. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

25. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

26. A semiconductor processing method comprising forming two series of field effect transistors over a substrate, at least one series being isolated from adjacent devices by shallow trench isolation, and further comprising achieving different threshold voltages between field effect transistors in different series by varying the active area widths of the field effect transistors in the series, at least one series having active area widths less than one micron.

27. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant.

28. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

29. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

30. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

31. A semiconductor processing method of forming dynamic random access memory circuitry comprising:

providing a substrate having a memory array area over which memory circuitry is to be formed, and a peripheral area over which peripheral circuitry is to be formed;

forming a plurality of shallow trench isolation regions received within the peripheral area of the substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different; and

forming a conductive line over respective active areas to provide individual transistor gates, the transistors corresponding to the active areas having the different widths having different threshold voltages.

32. The semiconductor processing method of claim 31 further comprising for the transistors having the different widths, providing the different threshold voltages without using a separate channel implant for the transistors.

33. The semiconductor processing method of claim 31, wherein the two different widths are each less than one micron.

34. A transistor assembly comprising:

a plurality of active areas having widths defined by shallow trench isolation regions of no greater than about one micron, at least some of the widths being different; and

gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another.

35. The transistor assembly of claim 34, wherein the threshold voltages of at least some of the individual transistors are less than one volt.

36. The transistor assembly of claim 34, wherein individual transistors having active areas with the smaller widths have threshold voltages which are smaller than other individual transistors having active areas with larger widths.

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37. The transistor assembly of claim 34, wherein one of the transistors comprises a portion of precharge circuitry for dynamic random access memory circuitry.

38. The transistor assembly of claim 34, wherein one of the transistors comprises a pass transistor.

39. The transistor assembly of claim 34, wherein one of the transistors comprises a portion of sense amplifier circuitry for dynamic random access memory circuitry and has a lower threshold voltage V_{tl}.

40. The transistor assembly of claim 34, wherein some of the transistors are joined together in a parallel configuration.

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41. Dynamic random access memory circuitry comprising:

a substrate having a memory array area for supporting memory circuitry and a peripheral area for supporting peripheral circuitry;

a plurality of active areas within the peripheral area having widths defined by shallow trench isolation regions of no greater than about one micron, at least some of the widths being different; and

conductive lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another.

42. The dynamic random access memory circuitry of claim 41, wherein the threshold voltages of at least some of the individual transistors are less than one volt.

43. The dynamic random access memory circuitry of claim 41, wherein individual transistors having active areas with the smaller widths have threshold voltages which are smaller than other individual transistors having active areas with larger widths.

44. A transistor assembly comprising:

an active area; B

a plurality of spaced-apart shallow trench isolation regions received by the active area and defining active sub-areas therebetween, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width; and

a gate line extending over the one and the other sub-area and defining, in part, separate transistors, wherein the separate transistors have different threshold voltages.

45. The transistor assembly of claim 44, further comprising a gate line extending over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron.

46. The transistor assembly of claim 44, further comprising a gate line extending over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron, wherein more than two of the plurality of transistors have different threshold voltages.

47. The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron.

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48. The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron and said plurality of transistors being joined in a parallel configuration.

49. A transistor assembly comprising:

an active area;

a plurality of spaced-apart shallow trench isolation regions received by the active area and defining active sub-areas therebetween, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is less than the one width; and

a gate line extending over the one and the other sub-area and defining, in part, separate transistors, wherein the separate transistors have different threshold voltages, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron and said plurality of transistors being joined in a parallel configuration to provide a pull down circuit coupled to a common node.

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50. The transistor assembly of claim 49, further comprising a sense amplifier formed from pair of transistors, each of the pair having a gate that is cross-coupled to a drain of another of the pair, sources of the pair being coupled to the common node.

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